

LA36100

Logic Analyzer



Features

- Large scale integrated circuit, FPGA, SOPC, high speed and large memory
- Perfect function of start, trigger and delay to track and take the concerned data effectively
- 32 data sampling channels, 2 external clock channels
- A fast and effective debugging tool for hardware and software of MCU
- 5.7' color LCD display, the resolution 320 x 240 points
- USB Device and RS232

Technical Specifications

INPUT		
Input Channel		32 data sampling channels, 2 external clock channels.
Threshold Voltage		6 independent and adjustable threshold voltages. Adjustable Range : -6V ~ +6V. Resolution : 0.1V.
Input Impedance		R >100 kΩ, C <8 pf.
SAMPLE / MEM	ORY	
Sampling Rate	Timing Rate	1Hz ~ 100MHz (Period 10ns ~ 1s), Resolution:10ns.
	State Rate	1Hz ~ 35MHz.
Sampling Phase		Rise edge, Fall edge.
Memory Depth		256k bytes / channel.
TRIGGER		
Trigger Condition		32 bits trigger level, 32 bits trigger comparand.
Event Count		1 ~ 999.
Memory Delay		1 ~ 260000 sampling cycles.
PATTERN GEN	ERATOR	
Pattern Type		CH00 ~ CH15 are counters with adding 1. CH16 ~ CH29 are shift pulse. CH30 ~ CH31 monitor external clk1 and clk2.
Pattern Rate		Frequency : 1Hz ~ 50MHz (period 20ns ~ 1s), resolution : 10 ns.
GENERAL CHA	RACTERISTICS	
Power		AC 220V (1±10%), 50Hz (1±5%), <u><</u> 10VA.
Display		5.7' TFT LCD.
Dimension		329 x 283 x 155 mm.
Weight		4.3 Kg.

WE PURSUE APOLICY OF CONTINUOUS DEVELOPMENT AND PRODUCT IMPROVEMENT. THUS THE SPECIFICATIONS IN THIS DOCUMENT AND THE LOCATION OF CONTROLS ON THE FRONT PANEL MAY BE CHANGED WITHOUT NOTICE.

Test & Measurement Instruments Division

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